known as the processor's instruction set. A processor's instruction set and how the instruction set is used to achieve a certain result are referred to as the processor's instruction set architecture ("ISA"). The processor's ISA also necessarily describes much of the processor's internal architecture. The assembly language instructions of a processor's instruction set internally access data of a defined size commonly known as a word. The word size of a processor is defined by the processor's ISA. Earlier personal computers, for example, the IBM PC sold by International Business Machines of Armonk, New York included a processor (the 8086) manufactured by Intel Corporation of Santa Clara, California which had a word size of 16 bits. As the personal computer has evolved, processing power has increased by, among other things, increasing the word size of a processor. Increasing the word size allows a processor to process more data in a shorter amount of time. Many current personal computers implement 32 bit word ISAs, while future personal computers will be implementing 64 bit word ISAs. Larger computers such as mainframes have ISAs with larger word sizes while smaller devices such as hand held personal digital assistants and cellular telephones have smaller word sizes.

On page 6, please amend the paragraph beginning on line 2 as follows:

The present invention relates to efficiently providing floating-point mathematical capabilities in a processor that supports two instruction set architectures. As increased use is being made of floating-point capabilities of a processor, processors are being designed to provide better floating-point support and increased floating-point performance. When creating a new processor with a new ISA to improve on existing technology, older instruction sets and ISAs may be supported to provide compatibility with software written for older processors. Such backward compatibility is commonly referred to as "legacy" support. When implementing a multi-mode processor that supports two different ISAs, certain functionality included in one ISA, typically the newer ISA, is not included in the other ISA, typically the older ISA. Pertinent to this invention is the sharing of floating-point components in a multi-mode processor that supports two different ISAs and, in particular, when the newer ISA provides a feature that is not supported by and/or interferes with concurrent implementations of the older ISA.